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10EC/TE71

Seventh Semester B.E. Degree Examination, Dec.2013/Jan.2014
Computer Communication Networks

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. How do the layers of TCP/IP model correlate to the OSI model? **(08 Marks)**
b. Explain about I × Cs with a schematic. What are Point of presence? **(06 Marks)**
c. How ADSL could achieve higher data rate over existing local loops? Explain DSLAM. **(06 Marks)**

2 a. With a frame format, give an elaborate account on HDLC. **(08 Marks)**
b. What is ARQ? Describe in detail about Go-Back-N ARQ. **(08 Marks)**
c. Explain Bit Stuffing with an example. **(04 Marks)**

3 a. With a flow diagram, explain CSMA/CD. **(08 Marks)**
b. What is channelization? Give a brief account on CDMA. **(08 Marks)**
c. What are the reasons for poor channel utilization in ALOHA systems? How the same is improved in CSMA? **(04 Marks)**

4 a. What are the reasons for not implementing CSMA/CD in wireless LANs? With a flowchart and frame exchange time line diagram, explain CSMA/CA. **(08 Marks)**
b. What are the advantages of having a Bridged Ethernet? **(06 Marks)**
c. List goals of the Fast Ethernet. Enumerate Fast Ethernet implementations. **(06 Marks)**

PART – B

5 a. List different connecting devices on the basis of layers they operate. **(04 Marks)**
b. Discuss about looping problem in transparent bridges. How spanning trees help avoid looping problem? **(08 Marks)**
c. What are virtual LANs? What is the basis for membership in VLAN? Enumerate advantages of having VLANs. **(08 Marks)**

6 a. Write a detailed account on IPv6 addresses. Expand the address 0:15::1:12:1213. **(10 Marks)**
b. Explain fields pertaining to Fragmentation in IPv4 header. **(06 Marks)**
c. In an IPv4 packet the value of HLEN is 5 and the value of the total length field is 0 × 0028. How many bytes of data are being carried by this packet? **(04 Marks)**

7 a. Compare multicasting and multiple unicasting. Discuss multicast distance vector routing. **(10 Marks)**
b. What are autonomous systems? Categorize autonomous systems. Give a brief note on BGP sessions. **(06 Marks)**
c. Mention the different fields in a typing routing table. What are the significance of Flags filed? **(04 Marks)**

8 a. Explain connection establishment and connection termination in TCP. **(10 Marks)**
b. Give user datagram format. List uses of UDP. **(06 Marks)**
c. What s FQDN? What is the need for DDNS? **(04 Marks)**

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10EC/TE72

Seventh Semester B.E. Degree Examination, Dec.2013/Jan.2014
Optical Fiber Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Describe block diagram of an optical fiber transmission link and explain the function of each element in link. **(08 Marks)**

b. Explain what is meant by graded index optical fiber using simple ray theory concept indicate the major advantages of this type of fiber with regard to multimode propagation. **(06 Marks)**

c. A Graded index fiber with parabolic refractive index has $n_1 = 1.48$ and $n_2 = 1.46$ if core radius is 20 μm. Find the number of modes at 1300nm and 1550 nm. **(06 Marks)**

2 a. Describe Rayleigh Scattering in optical fiber. **(06 Marks)**

b. Briefly explain intramodal and intermodal dispersion. **(06 Marks)**

c. Glass fiber exhibits material dispersion given by, $\lambda^2\left(\frac{d^2n_1}{d\lambda_2}\right)$ of 0.025. Determine material dispersion parameter at a wavelength of 0.85 μm and estimate rms pulse broadening / km for good LED source with an rms spectral width of 20 nm at this wavelength. **(08 Marks)**

3 a. Sketch and explain Fabry perot resonator cavity of laser. **(07 Marks)**

b. Discuss the operation of silicon RAPD with neat diagram. **(07 Marks)**

c. Consider a photodiode with quantum efficiency 75%, when photon of energy 1.6×10^{-19} J, are incident on the surface then calculate operating wavelength and if 2.6 μA photo current through detector corresponding, determine incident optical power when detector is operated at same wavelength. **(06 Marks)**

4 a. Describe with aid of suitable diagram, three common technique used for mechanical splicing of optical fibers. **(06 Marks)**

b. With aid of simple sketches, outline major categories of fiber couplers. **(06 Marks)**

c. A GaAs optical source that has a refractive index of 3.6 is closely coupled to step index fiber which has a core refractive index of 1.465, if the source size is smaller than fiber core, and small gap between source and fiber is filled with a gel that has a refractive index of 1.305. What is the power loss in decibels from source into fiber? **(08 Marks)**

PART – B

5 a. Briefly discuss the possible sources of noise in optical fiber receivers. **(06 Marks)**

b. Discuss how the eye diagram is powerful measurement tool for assessing the data handling capability in digital transmission system. **(08 Marks)**

c. Write a note on analog receivers. **(06 Marks)**

6 a. Explain the multi AM techniques employed in broadband analog application. **(08 Marks)**

b. Explain : (i) Microwave photonics (ii) RF over fiber. **(06 Marks)**

c. Explain in brief : (i) Short wavelength band (ii) Chirping. **(06 Marks)**

7 a. Explain the design and operation of polarization independent isolator. How it is different from polarization dependent isolator. **(06 Marks)**

b. Write a note on MEMS technology. **(06 Marks)**

c. Explain operational principle and implementation of WDM with diagrams. **(08 Marks)**

8 a. Write basic applications and types of optical amplifiers. **(08 Marks)**

b. Explain with the aid of neat diagram, three possible EDFA configurations. **(06 Marks)**

c. Describe SONET / SDH frame formals
SONET / SDH frame rings. **(06 Marks)**

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10EC73

Seventh Semester B.E. Degree Examination, Dec.2013/Jan.2014
Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Draw the circuit diagram, and control characteristics of GTO, MCT and BJT. **(06 Marks)**

b. What are power Electronic circuits? Explain any two of them with circuit, input and output waveforms. **(06 Marks)**

c. What are the peripheral effects of power electronic equipments and mention the remedies? **(05 Marks)**

d. What are the applications of power MOSFET's? **(03 Marks)**

2 a. Mention the merits and demerits of power MOSFET's. **(04 Marks)**

b. Draw the transient model of BJT and explain the switching characteristic of bipolar transistor. **(08 Marks)**

c. What is the need of base drive control and in a power transistor? Explain anti saturation control. **(08 Marks)**

3 a. Explain the two transistor model of thyristor and derive an expression for anode current interms of current amplification factor and leakage current. **(08 Marks)**

b. For the thyristor circuit shown in Fig.Q.3(b), the SCR has a latching current of 50mA and is fixed by a pulse of length 50μsec. Show that without resistance R, the thyristor will fail to remain on, when the firing pulse ends and then find the maximum value of R to ensuring firing. **(06 Marks)**

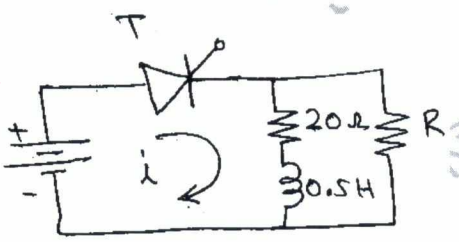


Fig.Q.3(b)

c. Design a UJT relaxation trigger circuit for SCR with V_{BB} = 20V, η = 0.6, I_p = 10μa, V^v = 2V and I_V = 10mA. The frequency of oscillation is 100Hz and triggering pulse width should be 50μsec. **(06 Marks)**

4 a. With the circuit and waveform, explain the operation of a single phase semi converter with inductive load. **(08 Marks)**

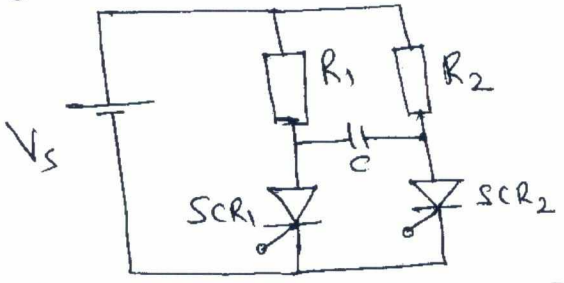
b. A single phase full converter is operated from a 120V, 60Hz supply. The load current with an average of I_a is continuous with negligible ripple current. If the delay angle is $\alpha = \frac{\pi}{3}$, calculate: i) Harmonic factor; ii) Displacement factor; iii) Power factor. **(07 Marks)**

c. What are the advantages of 1 - ϕ dual converter operation with circulating current. **(05 Marks)**

PART – B

5 a. Compare natural and forced commutation. **(05 Marks)**

b. Determine the proper values of the commutating components for the circuit shown in Fig.Q.5(b). The load current to be commutated is 5A, turn off time is 50μsec, supply voltage is 100V and SCR_2 holding current is 2mA. **(07 Marks)**



c. With the necessary circuit diagram and waveform, explain the operation of a complementary commutation. **(08 Marks)**

6 a. What are the applications of AC voltage controller? **(04 Marks)**

b. For the AC voltage controller shown in Fig.Q.6(b), calculate the average power in the lad if the thyristor firing angle is fixed at 45° with respect to supply voltage. Derive the necessary equation. **(08 Marks)**

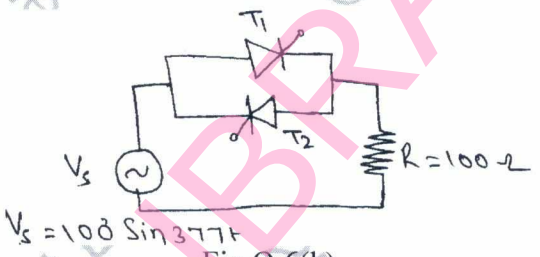


Fig.Q.6(b)

c. Explain the operation of a 1-ϕ controller with inductive loads and derive the expression of rms value of the output voltage. **(08 Marks)**

7 a. What are the applications of DC choppers? **(04 Marks)**

b. A DC chopper has a resistive load of 20Ω and input voltage 220V. When the chopper is on its voltage drop is 1.5V and chopping frequency is 10kHz. If the duty cycle is 80%, determine the average output voltage, rms value of the output voltage and chopper on time. **(07 Marks)**

c. Explain the operation of a step down chopper with RL load and also derive an expression of peak-peak output ripple current. **(09 Marks)**

8 a. Compare voltage source inverter and current source inverter. **(05 Marks)**

b. Explain the following performance parameters of a inverter:

i) Harmonic factor of nth harmonic.

ii) Total harmonic distortion.

iii) Distortion factor. **(06 Marks)**

c. The single phase full bridge inverter has a resistive load of R = 24Ω and the DC input voltage of V_s = 48V. Determine:

i) Rms output voltage at the fundamental frequency.

ii) Output power.

iii) Peak and average currents of each transistor. **(09 Marks)**

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10EC74

Seventh Semester B.E. Degree Examination, Dec.2013/Jan.2014

Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain: i) Embedded system, ii) Hard RTS, iii) Watch Dog Timer, with an example for each. **(06 Marks)**

b. With a block diagram, explain briefly the various components in a microprocessor based embedded system. **(06 Marks)**

c. Differentiate between the two design approaches for an embedded system development. Explain the various stages with a flow diagram. **(08 Marks)**

2 a. Compare:
i) Big Endian and Little Endian formats.
ii) RISC and CISC registers.
iii) Truncation and rounding errors. **(06 Marks)**

b. Explain direct and register indirect addressing modes with diagrams. Also write the timing diagram for a serial write operation with an 8 bit register. **(06 Marks)**

c. Write the block diagram of RTN model for a microprocessor data path and memory interface. Also explain fetch, execute and next control operations with RTL instructions. **(08 Marks)**

3 a. Explain the internal diagram of SRAM and write the timing diagram for read operation. **(06 Marks)**

b. Explain associative mapping cache implementation. **(06 Marks)**

c. Write the inside and outside diagrams for DRAM along with read and write operations. Also explain refresh operation. **(08 Marks)**

4 a. Write the flow diagrams for waterfall and V life cycle models and briefly explain Waterfall steps. **(06 Marks)**

b. Explain the characterizing and identifying the requirements of a system with respect to a digital counter. **(06 Marks)**

c. Write the hardware architecture and data and control flow diagram of a counter system and explain briefly the flow diagram. **(08 Marks)**

PART – B

5 a. Differentiate between:
i) Program and process;
ii) Processes and threads;
iii) Lightweight and heavy weight threads **(06 Marks)**

b. Describe:
i) Reentrant code,
ii) Foreground/background system,
iii) Multithreading system. **(06 Marks)**

c. Describe the task state transition with a diagram and TCB structures. Explain the function of the scheduler and also dispatcher. **(08 Marks)**

6 a. Explain any 6 functions of an operating system in brief. **(06 Marks)**

b. Describe virtual model and high level model for OS architectures. **(06 Marks)**

c. Write the algorithm for a simple OS Kernel, using C language notation for 3 asynchronous tasks using TCBs only. The 3 tasks use a common data buffer for read, increment and display operations. **(08 Marks)**

7 a. Write the Amdahl's law limitation for performance improvement/optimization. Consider a system with the following characteristics.

i) The task to be improved takes 200 time units and the gral is to reduce the execution time to 160 time units. The algorithm under consideration takes 80 time units. Determine the unknown parameter value in the equation and write the inference.

ii) If the goal is to reduce the execution time to 100 time units for the values in case(i), then determine the value unknown parameter value in the equation and write the inference.

(06 Marks)

b. Write a 'C' function to determine the sum of the elements in an array and analyze it line by line for its time complexity **(06 Marks)**

c. Explain the Big-O notation used for comparing the algorithms, common bounds used with a table, graph and rules used for Big-O arithmetic. **(08 Marks)**

8 a. Write and analyze a linear search algorithm for its time complexity. **(06 Marks)**

b. The operation to be performed is (i) c = a + b, (ii) c = d +e if a = = b else c = d – e. Write the C language construct and assembly language statements for the above 2 cases separately and calculate the total time required if PUSH/POP takes 800 nsec, arithmetic operation/load/store/cmp takes 400 nsec and the conditional/unconditional branch takes 700 nsec. **(06 Marks)**

c. Describe memory loading with equation, figure and an example. **(08 Marks)**

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10EC751

Seventh Semester B.E. Degree Examination, Dec.2013/Jan.2014
DSP Algorithms & Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With the help of block diagram, explain decimation and interpolation process. Use necessary equations. **(06 Marks)**

b. The signal sequence $x(n) = (0, 4, 8, 12, 16)$ is interpolated using the interpolation filter sequence $b_K = \left\{\frac{1}{4}, \frac{2}{4}, \frac{3}{4}, 1, \frac{3}{4}, \frac{2}{4}, \frac{1}{4}\right\}$ and the interpolation factor is 2. Determine the interpolated sequence y(m). **(06 Marks)**

c. Explain with the help of block diagram DSP system. Draw the timing diagram. **(08 Marks)**

2 a. Give the structure of a 4×4 Braun multiplier and explain its concept. What is the need of Bangh Wooley multiplier? **(06 Marks)**

b. Explain the Guaad bits in a MAC unit of a DSP. Consider a MAC unit whose inputs are 24-bit numbers. How many Guard bits should be provided if 512 products have to be added in the accumulator to prevent overflow condition? What is the overall size of the accumulator required? Draw the figure. **(06 Marks)**

c. Explain the circular and bit reversed addressing mode with the help of algorithm. **(08 Marks)**

3 a. List the architectural features of three fixed point DSPs. **(06 Marks)**

b. Draw the functional diagram of the barrel shifter of TMS 320C54XX processor and explain its working. **(06 Marks)**

c. Show all the bits of program mode status register and explain the functions of following bits: $MP/\overline{MC}$, OVLY, DROM. **(04 Marks)**

d. Assuming the current contents of AR_3 to be 0200H, what will be its contents after each of the TMS320C54XX addressing modes is used. Assume that the contents of AR_0 are 20 H:
(i) $*AR_3 + OB$ (ii) $*AR_3 - OB$ **(04 Marks)**

4 a. Show the pipeline operation of the following sequence of instructions and if the initial value of AR_3 is 80H and the values stored in memory location 80, 81, 82 are 1, 2 & 3.

```
LD *AR3+, A
ADD #1000H, A
STL A, *AR3+
```

(06 Marks)

b. With neat sketch explain the logic block diagram of a timer circuit. **(06 Marks)**

c. Write a program to find the sum of a series of signed numbers stored at successive locations in the data memory and place the result in the accumulator.

$$A = \sum_{i=410H}^{41FH} dmad(i)$$

Use AR_1 as a pointer and AR_2 as a counter for the numbers. **(08 Marks)**

PART – B

5 a. What do you mean by Q notation used in DSP algorithm implementation? What are the values represented by 16-bit number N = 4000H in Q_{15} and Q_7 notation? **(06 Marks)**

b. Briefly explain IIR filters. With the help of block diagram, explain second order IIR filter. **(06 Marks)**

c. Write a TMS320C54XX program that illustrates the implementation of an interpolating FIR filter of length 15 and interpolating factor 5. **(08 Marks)**

6 a. Write TMS320C54XX program for 8-point FFT implementation structure. **(12 Marks)**

b. With the help of algorithm generate bit reversed index for 16-point DFT computation. **(08 Marks)**

7 a. Design a circuit to interface 4K×16 and 2K×16 memory chips to realize program memory space for TMS320C54XX DSP in the address range 03F000H – 03FFFFH and 05F800H – 05FFFFH respectively. Plot the memory mapping. **(12 Marks)**

b. Draw the flow chart of the interrupt handling by the TMS320C54XX processor and explain handling of interrupts. **(08 Marks)**

8 a. With a neat block diagram and timing diagram for both transmit and receive operation, explain the signals involved in synchronous serial interface. **(12 Marks)**

b. With the help of block diagram, explain the clipping autocorrelation pitch detector. **(08 Marks)**

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10EC762

Seventh Semester B.E. Degree Examination, Dec.2013/Jan.2014
Real Time Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Classify RTS based on time constraints. **(06 Marks)**

b. Explain the following:
i) Clock based tasks.
ii) Event based tasks.
iii) Interactive systems. **(06 Marks)**

c. Explain the following programs: i) Sequential; ii) Multitasking; iii) Real time. **(08 Marks)**

2 a. With neat sketch, explain sequence control for a single chemical reactor vessel. **(07 Marks)**

b. With neat diagram, explain loop control and list the advantages of loop control over analog control. **(07 Marks)**

c. Write a note on distributed systems. **(06 Marks)**

3 a. Explain with neat sketch, digital input interface. **(07 Marks)**

b. With neat diagram, explain the block diagram of general purpose computer. **(07 Marks)**

c. Explain with neat sketch communications and give the ways of characterizing serial communication techniques. **(06 Marks)**

4 a. Explain the following terms: i) Security; ii) Readability; iii) Portability. **(09 Marks)**

b. Explain the following data types:
i) Sub range type; ii) Derived types. **(05 Marks)**

c. Explain: i) Exception handling; ii) Coroutines. **(06 Marks)**

PART – B

5 a. Explain scheduling strategies. **(06 Marks)**

b. Explain priority structures. **(06 Marks)**

c. List the functions of task management. Explain with a neat diagram task state diagram and task states. **(08 Marks)**

6 a. Explain task chaining and swapping. **(06 Marks)**

b. Explain: i) Serially reusable code; ii) Reentrant code. **(08 Marks)**

c. What is liveness? Explain. **(06 Marks)**

7 a. Explain software design related to preliminary design of RTSS with neat diagram. **(06 Marks)**

b. With flow chart explain foreground/background approach. **(08 Marks)**

c. Explain multitasking approach. **(06 Marks)**

8 a. Explain Yourdon methodology. **(05 Marks)**

b. Explain the context diagram for drying oven in case of Ward and Mellor method. **(08 Marks)**

c. Differentiate between Ward and Mellor and Hatley and Pirabhai methodologies. **(02 Marks)**

d. Explain architecture model with neat diagram in case of Hatley and Pirabhai method. **(05 Marks)**

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.